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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional)	
		TESSERA 3.0-205 A DIV	
	Application Number	Filed	
	10/648,002-Conf. #3311	August 26, 2003	
	First Named Inventor		
Masud Beroz, Belgacem Haba, and Klaus-jurgen Wolter			
Art Unit		Examiner	
3729		M. N. Trinh	
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <p><input type="checkbox"/> applicant /inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>51,773</u></p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____</p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p> <p><input type="checkbox"/> *Total of <u>1</u> forms are submitted.</p>			



Signature

Matthew E. Hanley

Typed or printed name

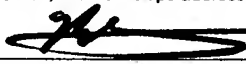
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February 10, 2006

Date

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: February 10, 2006 Signature:  (Matthew E. Hanley)

Claims 5-9 stand rejected under 35 U.S.C. 102(e) on DiStefano, U.S. Patent No. 6,044,548 ("DiStefano") and are the subject of this request for review. Of these, claim 5 is the sole independent claim. For the reasons set forth below, applicants believe that this rejection is clearly erroneous.

Claim 5.

Claim 5 discloses a method of bonding microelectronic elements to components. The method of claim 5 requires providing "a working space at least partially bounded by a deformable barrier" so that "conductive features of said microelectronic elements and components confront one another within" this working space. (claim paragraph (a)). These conductive feature are subsequently bonded to one another by a "bonding material" (claim paragraph (c)). This element is not present in the cited prior art.

One example of the method recited in claim 5 is depicted in Fig. 13 of the application, wherein the microelectronic elements 510 and component 530 are placed on a fixture and a deformable barrier 590 in the form of a flexible film is disposed over the rear surfaces of the microelectronic elements and the fixture, forming a working space 594.

Distefano is directed to a method of joining a semiconductor chip to a connection component using physical pressure and an adhesive film. In rejecting claim 5, the Examiner stated that Distefano discloses a working space in Figure 6 wherein the "working space is located where [support layer] 80 and [adhesive sealant] 88 reside." (Advisory Action dated 01/04/2006.) The Examiner also stated that "88 is a flexible film."

One deficiency in the rejection lies in the fact that the alleged flexible film pointed out by the Examiner, which is actually an adhesive sealant, *does not partially bound a working space* as specifically recited in claim 5. As depicted in Fig. 6

of Distefano, the adhesive sealant 88 pointed out by the Examiner is sandwiched between a connection component 90 and a semiconductor chip 92. The adhesive sealant is disposed in this location so that it can be brought to an elevated temperature, form a liquid adhesive, and solidify to form a substantially void-free interface between the chip and the connection component. (Col. 11, lines 42-65.) The adhesive layer serves to essentially glue the two components together, it does not define a working space.

Moreover, nothing in the rejection points out where conductive features of the microelectronic element and the component confront one another "within" any working space bounded by alleged flexible film 88. In DiStefano, the conductive features which are bonded to one another are the lead tips 58 (Fig. 4) and chip contacts 95. These features are not disposed "within" any space bounded by film 88; as clearly shown in Fig. 4, the lead tips project through this film.

Distefano additionally does not disclose maintaining a difference in absolute pressure between a working space and a space outside of the working space. The portion of Distefano relied upon by the Examiner merely suggests that the entire assembly shown in Fig. 6 should be "by squeezing it between a top platen 96 engaged with the top surface of sheet 32 and a bottom platen 98 engaged with the bottom surface of the chip [chip 92, Fig. 6]." (Col. 11, lines 21-24.) The layers are subjected to mechanical forces, there is no pressure differential created across any flexible film depicted in Fig. 6. Thus, Distefano fails to disclose this element of claim 5. The statement in the reference that this step may be performed "under vacuum" does not suggest otherwise; that statement suggests enclosing all of the elements shown in Fig. 6 in a conventional vacuum chamber; such an arrangement would not result in a pressure differential across any flexible film.

The same reasons apply with respect to claims 6-9.

Claim 6

As to claim 6, the rejection is additionally erroneous because the claim requires that the "deformable barrier" which is subjected to the pressure differential must be "a flexible film separate from" the elements to be joined in the process. All of the dielectric elements 32,80 and 88 shown in Fig. 6 of DiStefano are part of the component shown in Fig. 4. None could constitute the deformable barrier of claim 6.

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